Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.055”**

**.055”**

**NOTE: Chip back must be connected to V-**

**7**

**1**

**2**

**6**

**5**

**4**

**3**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: Z**

**APPROVED BY: DK DIE SIZE .055” X .055” DATE: 8/22/16**

**MFG: NATIONAL THICKNESS .015” P/N: LF351**

**DG 10.1.2**

#### Rev B, 7/1